

Resources for Measurement-Based Quantum Carry-Lookahead Adder



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Abstract

We present the design of a quantum carry-lookahead adder using measurement-based quantum computation. QCLA utilizes MBQC's ability to transfer quantum states in unit time to accelerate addition. The quantum carry-lookahead adder (QCLA) is faster than a quantum ripple-carry adder; QCLA has logarithmic depth while ripple adders have linear depth. QCLA is an order of magnitude faster than a ripple-carry adder when adding registers longer than 100 qubits but requires a cluster state that is an order of magnitude larger. Hand optimization results in a $\approx 13\%$ reduction in spatial resources for the circuit. Ideal optimization is $\approx 19\%$ [3].

Introduction

Measurement-based quantum computation (MBQC) is a new paradigm for implementing quantum algorithms using a quantum cluster state [1]. All gates in the Clifford group, including CNOT, can be performed in one time step via a large number of concurrent measurements. Remarkably, because both wires and SWAP gates are in the Clifford group, MBQC supports long-distance gates in a single time step. The Toffoli Phase gate can be executed in two time steps, where the measurement basis for the second step is selected depending on previous measurement outcomes. This adaptive process determines the overall performance of many algorithms.

The performance and requirements for the MBQCLA are evaluated. A direct mapping of the circuit model MBQC is given, followed by the optimization for the circuit. The optimization is done by removing the unnecessary wires between the quantum gates and compressing the spacing of active gates.

In order to obtain the performance and resource requirements of the circuit, we have calculated the execution time, circuit area, the number of qubits in the cluster state, and the number of clustering operations required to make that cluster state. The resources are specified in terms of n , the length of each of the registers to be added, in qubits.

The area is the height of the cluster state multiplied by the width, measured in cluster state lattice sites. The depth of the circuit is the number of time steps required to execute the circuit, counted in qubit measurements.

Our goal is to minimize execution time while the other three are measures of the cost. The circuit needs to be separated into two type of resources: **computational resources** include NOT, CNOT, and Toffoli Phase Gates. Second, **communication resources** are the required for SWAP gate and wires. An optimal circuit is one which contains no communication resources, only computational gates. Thus, ideal optimization

is defined by the resources subtraction of the unoptimized MBQCLA by the sum of computational and vertical resources[3].

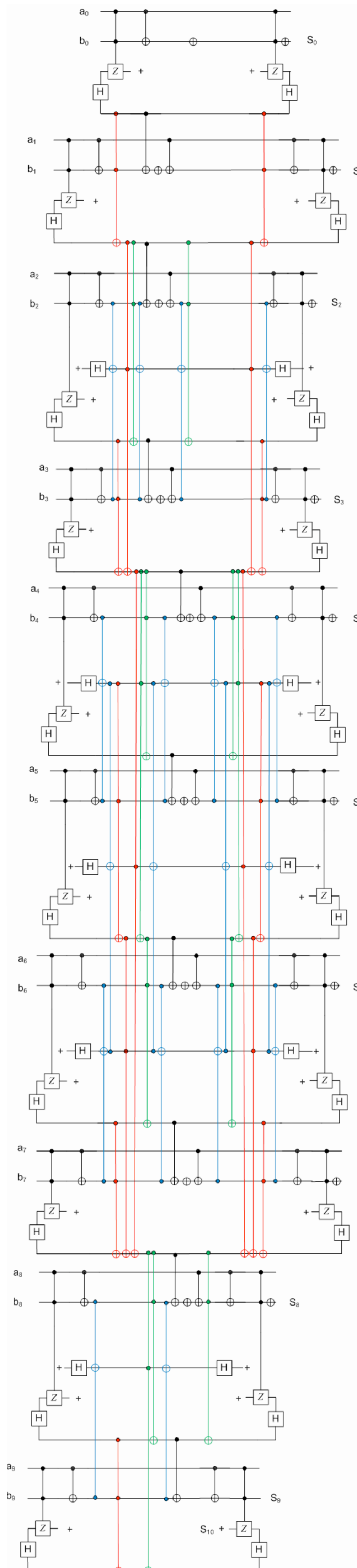


Figure 1. Optimized in-place circuit. Low $n-1$ bits of the carry string output are tucked into the interior of the circuit by bending the network[1,2].

• A carry-lookahead adder uses three phases, the "Generate" (G, blue color), "Propagate" (P, red color), and "Kill" (K) networks, each of which progressively doubles the length of its span in each time step to calculate the complete "Carry" values (C, green color). In practice, the networks are somewhat redundant, and Draper et al. defined their circuit using only the P and G networks to calculate the final carry C. The out-of-place form of the QCLA performs the unitary transformation

$$|a, b, 0\rangle \rightarrow |a, b, a+b\rangle \text{ and the in-place form calculates}$$

$$|a, b\rangle \rightarrow |a, a+b\rangle \text{ where } |a\rangle, |b\rangle \text{ and } |a+b\rangle \text{ are } n\text{-qubit registers.}$$

• The implementation of these networks in reversible computation is realized by the following these steps where n as logical qubits, t is the round number and m is the index of qubits in the register:

1. P -rounds. For $t=1$ to $\lfloor \log n \rfloor - 1$: for $1 \leq m < \lfloor n/2^t \rfloor$. Then the connection between the round is expressed by: $P_t \oplus = P_{t-1}[2m]P_{t-1}[2m+1]$.
2. G -rounds. For $t=1$ to $\lfloor \log n \rfloor$: for $0 \leq m < \lfloor n/2^t \rfloor$. And, the connection between the round is: $G[2^t m + 2^t] \oplus = G[2^t m + 2^{t-1}]P_{t-1}[2m+1]$.
3. C -rounds. For $t = \lfloor \log 2n/3 \rfloor$ down to 1: for $1 \leq m < \lfloor (n-2^{t-1})/2^t \rfloor$. The connection between the round is expressed by: $G[2^t m + 2^{t-1}] \oplus = G[2^t m]P_{t-1}[2m]$.

• The procedures of in-place circuit is given by:

1. For $0 \leq i < n$, $Z[i+1] \oplus = A[i]B[i]$ setting $Z[i+1] = g[i, i+1]$.
2. For $0 \leq i < n$, $B[i] \oplus = A[i]$ setting $B[i] = p[i, i+1]$ for $i > 0$ and $B[i] = s_0$.
3. Run the circuit of P, G, and C networks sequences. Upon completion, $Z[i] = c_i$ for ≥ 1 .
4. For $1 \leq i < n$, $B[i] \oplus = Z[i]$. Now $B[i] = s_i$.
5. For $0 \leq i < n-1$, $\neg B$ contains s' .
6. For $1 \leq i < n-1$, $B[i] \oplus = A[i]$.
7. Run the P, G, and network in reverse then upon completion, $Z[i+1] = a_i s'_i$ for $0 \leq i < n-1$, and $B = a_i \oplus s'_i$ for $1 \leq i < n$.
8. For $1 \leq i < n-1$, $B[i] \oplus = A[i]$.
9. $0 \leq i < n-1$, $Z[i+1] \oplus = A[i]B[i]$.
10. $0 \leq i < n-1$, $\neg B$.

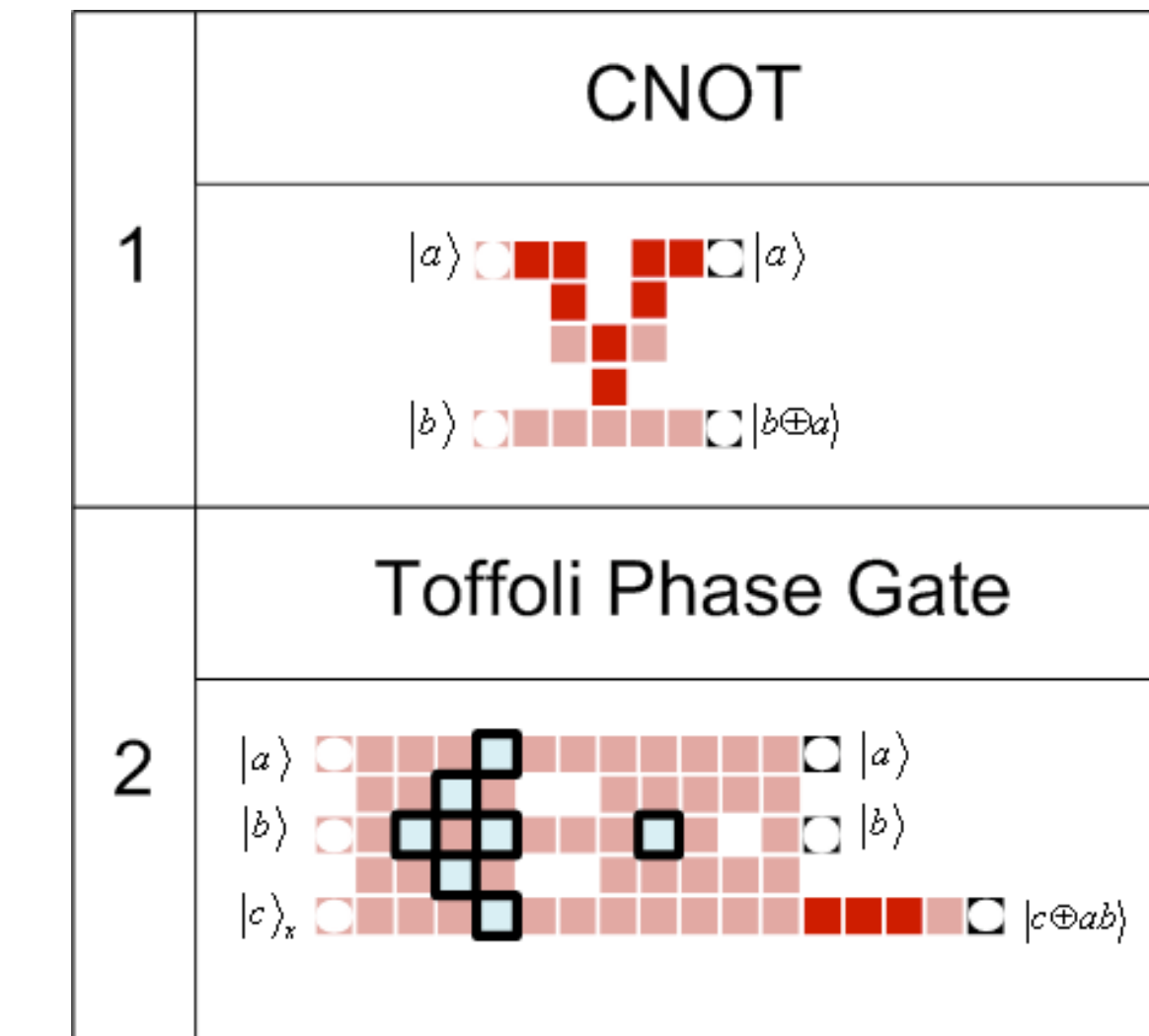


Figure 2. (a) Quantum gates in Measurement-Based Quantum Computation. Due to the relationship between CCNOT and Toffoli Phase Gate (TPG), $\text{CCNOT} = \mathbf{H}_t(\mathbf{TPG})\mathbf{H}_t$, the target qubit can be chosen arbitrarily by putting a Hadamard gate on the chosen qubit.

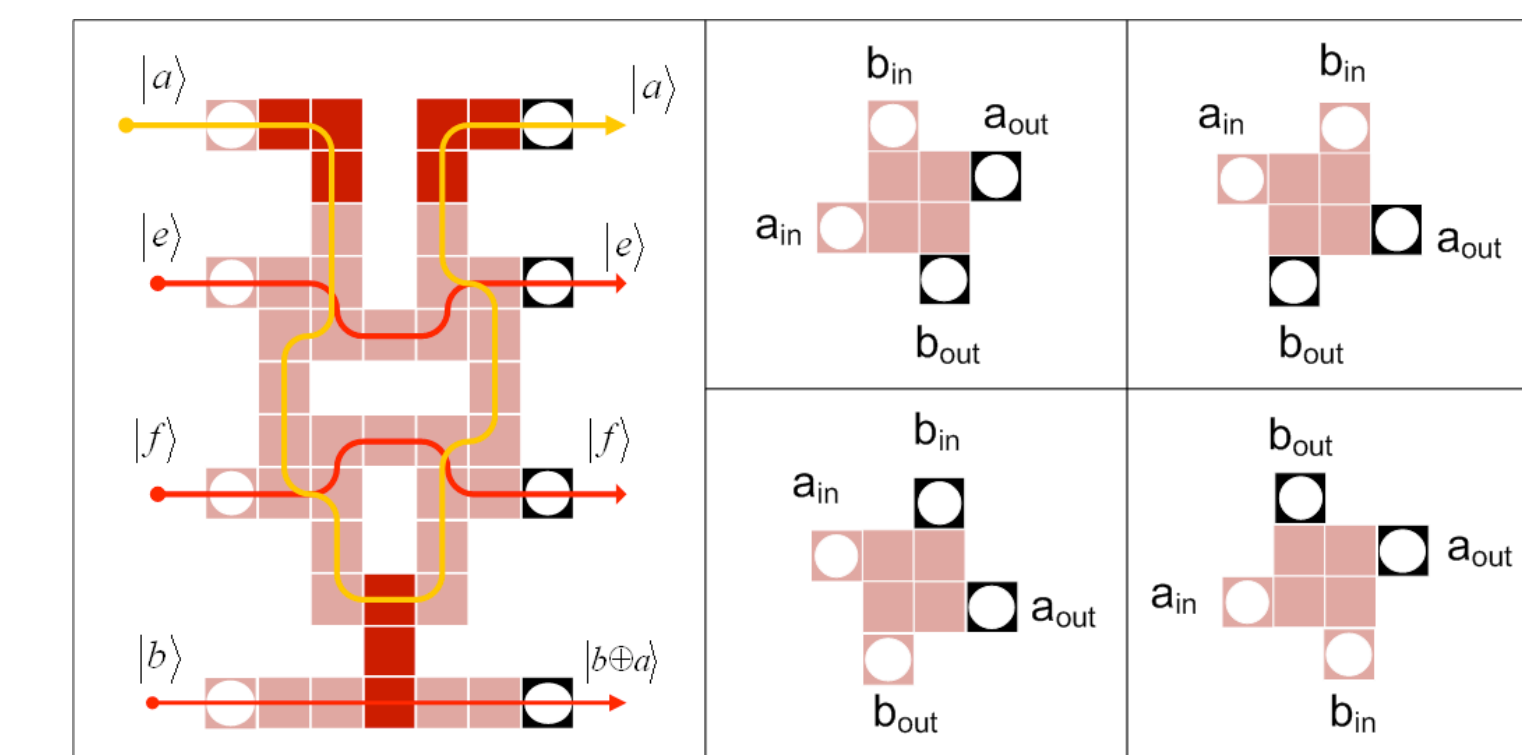


Figure 3. Non-adjacent computation. The implementation of four type SWAP gates to propagate the information up-to-down of non-adjacent qubits for performing CNOT. Qubit $|a\rangle$ acts as the control qubit and $|b\rangle$ is the target qubit.

Results

By considering the number of SWAP, Toffoli and CNOT gates in addition circuit and in P, G and C networks as shown above, we can approximate the physical resources needed for the out-of-place MBQCLA following this expression:

$$Size = \sum_i (Resources \text{ for } i - Gate)_i \approx \sum_i (A \times B \times T + D(C - E \times T))_i \quad (1)$$

where

$i \in \{\text{Toffoli Phase Gate, CNOT Gate, NOT Gate and SWAP Gate}\}$

A = number of logical qubits

B = number of rounds for the gate of type i

C = number of gates of type i

T = width of the i -gate (in lattice sites)

D = number of lattice qubits in an i -gate

E = number of logical qubits in an i -gate

The vertical communication resources (SWAP gates, especially) for (unoptimized) in-place MBQCLA circuit can be determined as follow:

$$\sum_{tp=1}^{\log_2[n]-1} \sum_{tg=1}^{\log_2(n)} \sum_{tc=1}^{\lfloor \log_2 \frac{2n}{3} \rfloor} 8n - 2w(n) - 2\lfloor \log_2(n) \rfloor + 2n - 2^{tp+1} + 4\lfloor \log_2(n) \rfloor + 2^{tg+1} \lfloor \log_2(tg) \rfloor + 2n - 2\lfloor \log_2(tc) \rfloor - 2 \quad (16a)$$

The mathematical expression of optimal in-place MBQCLA circuit can be determined by the sum of multiplication between quantum gates and their resources:

$$162(w(n) + \lfloor \log_2(n-1) \rfloor + \lfloor \log_2(n) \rfloor - w(n-1)) + 542n - 395$$

To optimize the circuit, we take small groups of qubits, or subregisters, and slide them toward the middle of circuit. Bending network can reduce the cluster resources required near qubits $a_0, a_1, a_2, a_3, a_4, a_6, a_8$, and a_9 by the amount:

$$\sum_i^n (C_i A_i W)$$

where

C_i = the number of rounds (columns) that i th-subregister moves.

A_i = number of logical qubits in the i th-subregister (usually 3, sometimes 4)

W = width of Toffoli Phase Gate

By the use of equations above, one can quantitatively obtain the design and size of circuit and also its optimization as given below:

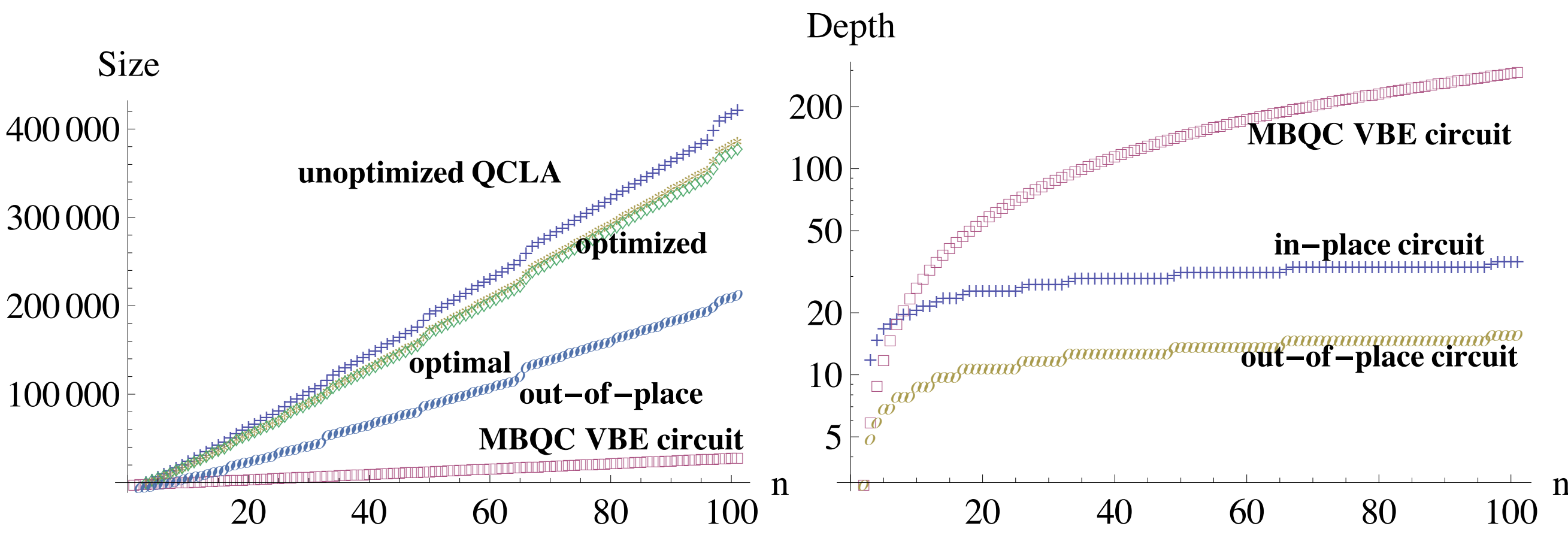


Figure 4. Size and depth comparison between MBQCVBE and MBQCLA. "+" and "◇" marks are for in-place, optimal, (by hand) optimized in-place, out-of-place and MBQCVBE circuits, respectively. In the right-hand graph, the data points for the optimized and optimal forms are almost indistinguishable.

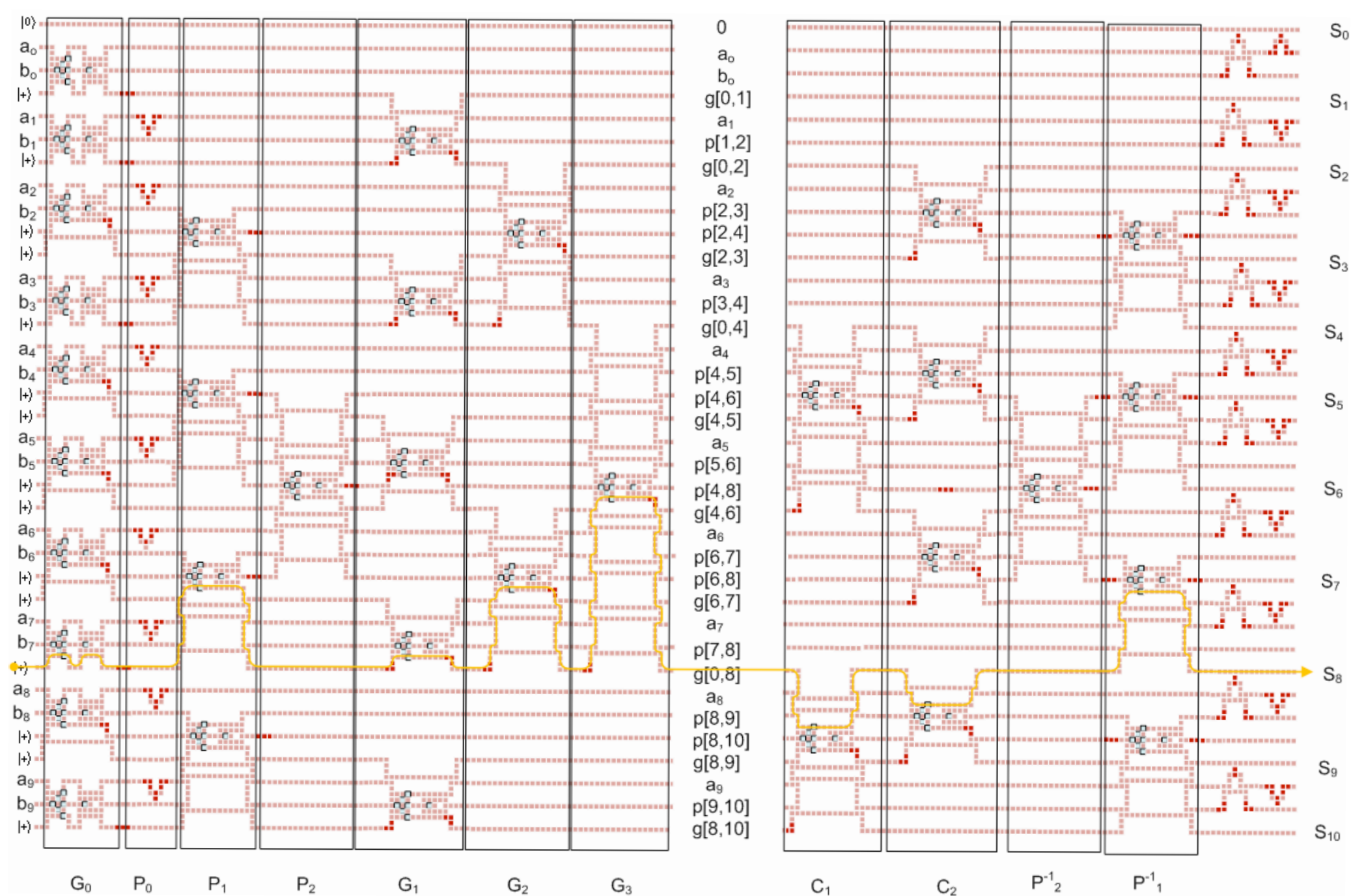


Figure 5. Out-of-place MBQCLA. For $n=10$, the circuit consists of: 4 addition blocks, 9 rounds of gates for the carry networks (2 Propagate, 3 Generate, 2 Inverse Propagate and 2 Carry networks).

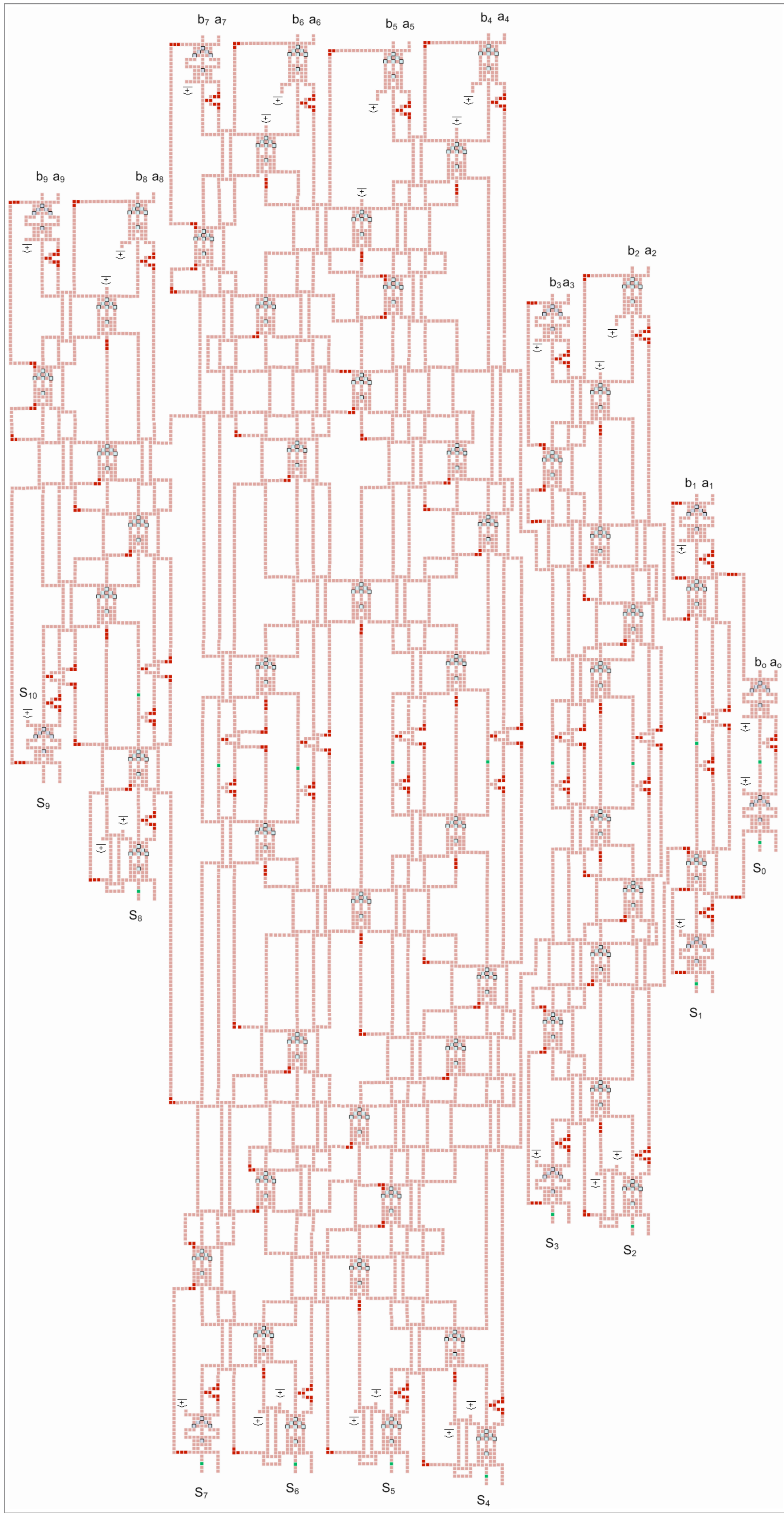


Figure 6. Optimized in-place MBQCLA circuit corresponding to diamond-like form circuit, spatial resources optimization by hand is $\approx 13\%$ from in-place MBQCLA circuit and $\approx 19\%$ for ideal condition [3].

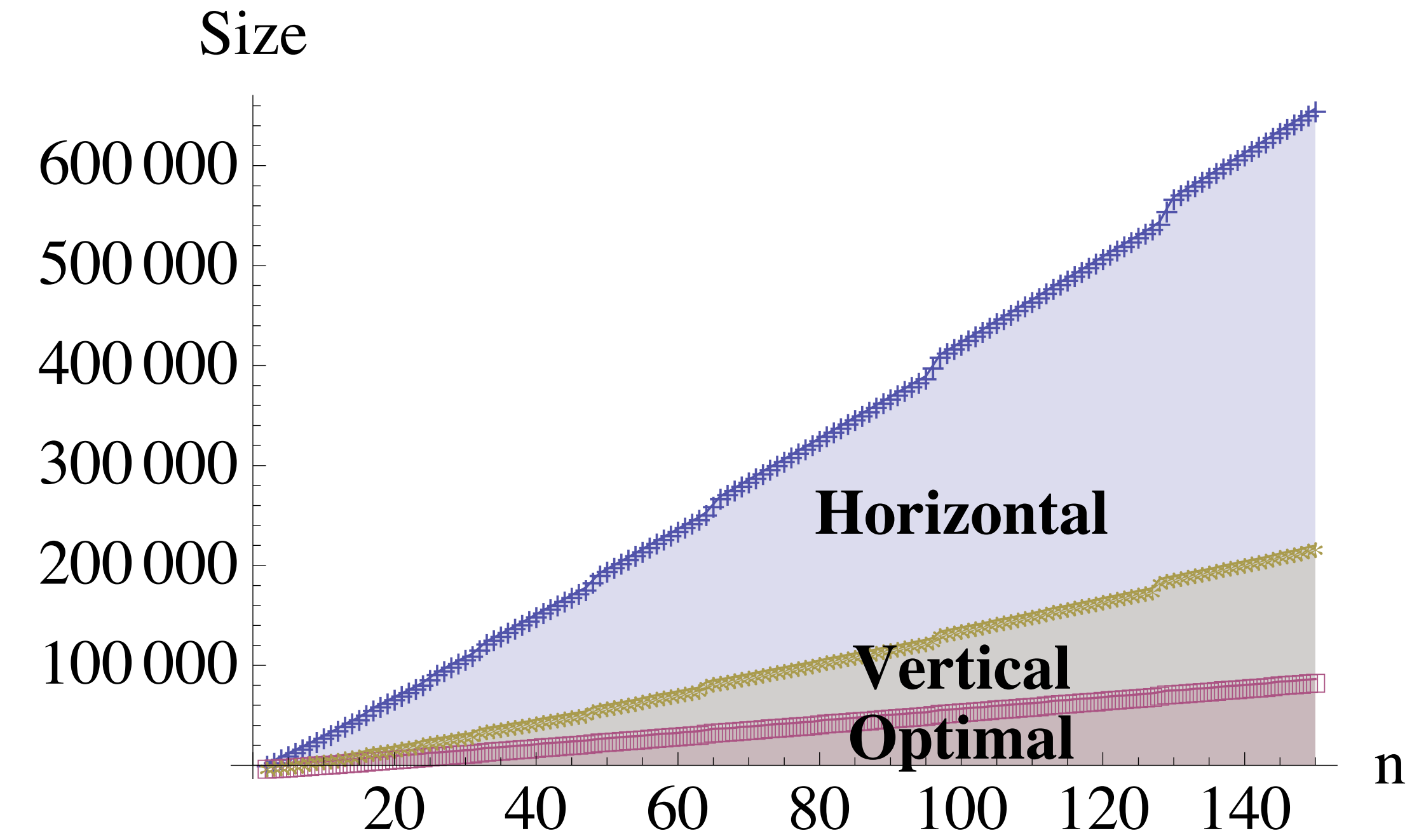


Figure 7. Resources comparison of optimal and un-optimal circuit. The bottom graph represents the ideal circumstance for optimal circuit and the other two show the circuit with additional resources for horizontal and vertical communications.

Conclusion

In our circuit, the depth is reduced to $\lfloor \log_2(n) \rfloor + \lfloor \log(n-1) \rfloor + \lfloor \log_2(n/3) \rfloor + \lfloor \log_2(n-1/3) \rfloor + 14$ for QCLA compared to $\approx O(n)$ for the ripple-carry. However, this circuit costs more in physical resources $\approx 2896n + 64n \lfloor \log_2(n) \rfloor$ compared to $\approx 304n$ for the ripple-carry[1][2]. The hand optimization of spatial resources in the circuit is $\approx 336n + 210w(n) + 14 \lfloor \log_2(n) \rfloor$ yielding $\approx 13\%$ reduction in spatial resources for MBQCLA circuit. This optimization results in a near-optimal circuit. Ideal optimization is $\approx 19\%$ [3].

References

- [1]. Robert Raussendorf, Daniel E. Browne, and Hans J. Briegel. Measurement-based quantum computation on cluster states. *Phys. Rev. A* 68, 022312 (2003).
- [2]. T. Draper, S. Kutin, E. Rains, and K. Svore. A Logarithmic-Depth Quantum Carry-Lookahead Adder. *QIC* 6 (4--5), 351-369 (2006).
- [3]. A. Trisetarso, R. Van Meter, and K. M. Itoh. Circuit Design for a Measurement-Based Quantum Carry-Lookahead Adder. Unpublished.